CLAIMS

The following is claimed:

1. A method of generating a boundary-scan description language file for an integrated circuit; comprising the steps of:

creating a flat netlist that describes said integrated circuit, wherein said flat netlist comprises connectivity information regarding leaf cells within said integrated circuit;

determining and storing a name provided for each joint test action group register located within said integrated circuit, from said created flat netlist;

determining relationships between each joint test action group register located within said integrated circuit and at least one input/output pin located within said integrated circuit, from said created flat netlist, and storing a description of said relationships; and

creating said boundary-scan description language file from said stored names of each joint test action group and said stored description of said relationship between said joint test action group register and said input/output pin.

2. The method of claim 1, wherein said step of creating a flat netlist further comprises the steps of:

traversing at least one hierarchical netlist that describes portions of said integrated circuit, for at least one individual netlist that describes a logic portion of said integrated circuit; and

combining connectivity information provided by said at least one individual netlist, resulting in said flat netlist.

3. The method of claim 2, wherein said connectivity information comprises relationships between wires within said integrated circuit, said leaf cells located within said integrated circuit and input/output pins.

4. The method of claim 2, wherein said joint test action group register names are stored in the same order discovered during said traversing step.

5. The method of claim 2, further comprising the step of:

traversing said at least one hierarchical netlist for at least one individual netlist that describes at least one pad located within said integrated circuit.

6. The method of claim 5, wherein said step of traversing said at least one hierarchical netlist is started at a beginning of a boundary-scan line, and wherein said step of traversing is ended at an end of said boundary-scan line.

7. The method of claim 1, wherein said joint test action group registers comprise a JO joint test action group register, a JT joint test action group register, and a JI joint test action group register.

8. A system for generating a boundary-scan description language file for an integrated circuit, comprising:

means for creating a flat netlist that describes said integrated circuit, wherein said flat netlist comprises connectivity information regarding leaf cells within said integrated circuit;

means for determining and storing a name provided for each joint test action group register located within said integrated circuit, from said created flat netlist;

means for determining relationships between each joint test action group register located within said integrated circuit and at least one input/output pin located within said integrated circuit, from said created flat netlist, and for storing a description of said relationships; and

means for creating said boundary-scan description language file from said stored names of each joint test action group and said stored description of said relationship between said joint test action group register and said input/output pin.

9. The system of claim 8, further comprising:

means for traversing at least one hierarchical netlist that describes portions of said integrated circuit, for at least one individual netlist that describes a logic portion of said integrated circuit; and

means for combining connectivity information provided by said at least one individual netlist, resulting in said flat netlist.

10. The system of claim 9, wherein said connectivity information comprises relationships between wires within said integrated circuit, said leaf cells located within said integrated circuit and input/output pins.

11. The system of claim 9, wherein said joint test action group register names are stored in the same order discovered during traversing.

12. The system of claim 9, further comprising means for traversing said at least one hierarchical netlist for at least one individual netlist that describes at least one pad located within said integrated circuit.

13. The system of claim 12, wherein said means for traversing said at least one hierarchical netlist begins traversing at a beginning of a boundary-scan line and ends traversing at an end of said boundary-scan line.

14. The system of claim 8, wherein said joint test action group registers comprise a JO joint test action group register, a JT joint test action group register, and a JI joint test action group register.

15. A system for generating a boundary-scan description language file for an integrated circuit, comprising:

a memory;

software stored within said memory defining functions to be performed by said system; and

a processor configured by said software to perform the steps of:

creating a flat netlist that describes said integrated circuit, wherein said flat netlist comprises connectivity information regarding leaf cells within said integrated circuit;

determining and storing a name provided for each joint test action group register located within said integrated circuit, from said created flat netlist;

determining relationships between each joint test action group register located within said integrated circuit and at least one input/output pin located within said integrated circuit, from said created flat netlist, and storing a description of said relationships; and

creating said boundary-scan description language file from said stored names of each joint test action group and said stored description of said relationship between said joint test action group register and said input/output pin.

16. The system of claim 15, wherein said step of creating a flat netlist further comprises the steps of said processor traversing at least one hierarchical netlist that describes portions of said integrated circuit, for at least one individual netlist that describes a logic portion of said integrated circuit, and said processor combining connectivity information provided by said at least one individual netlist, resulting in said flat netlist.

17. The system of claim 16, wherein said connectivity information comprises relationships between wires within said integrated circuit, said leaf cells located within said integrated circuit and input/output pins.

18. The system of claim 16, wherein said joint test action group register names are stored in the same order discovered during said traversing step.

19. The system of claim 16, wherein said processor is further configured by said memory to perform the step of traversing said at least one hierarchical netlist for at least one individual netlist that describes at least one pad located within said integrated circuit.

20. The system of claim 19, wherein said step of traversing said at least one hierarchical netlist is started at a beginning of a boundary-scan line, and wherein said step of traversing is ended at an end of said boundary-scan line.